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CLAIMS:

1.   A method for use in the manufacture of an integrated circuit, the method
comprising:
    -          providing a library of pre-designed specialized stream processing circuit
(10a-c) design data;
5   -   generating integrated circuit design data of an integrated circuit that
incorporates selected ones of the stream processing circuits (10a-c) at selected positions
along a stream processing chain in an integrated circuit, by including the stream processing
circuit design data substantially without modifying the stream processing circuit design data
(10a-c);
10 -   adding local control circuits (11) to the integrated circuit design, each coupled
to a control parameter input of a respective stream processing circuit (10a-c) that requires at
least one variable control parameter value, the local control circuits (11) being arranged to
control timing of control parameter updates by counting off block size dependent time
intervals between times points of successive control parameter updates;
15 -   adding a common control circuit (14) to the integrated circuit design, for
supplying instructions to the local control circuits (11), the instructions specifying block sizes
and parameter values.

2.   A method according to claim 1, comprising manufacturing an integrated
20 circuit according to the integrated circuit design data.

3.   A method according to claim 1, wherein at least one of the local control
circuits (11) has outputs coupled to control parameter inputs of a plurality of stream
processing circuits (10a-c) that operate using mutually common block sizes, the at least one
25 of the local control circuits timing updates of the control parameters of the plurality of stream
processing circuits in common.

4.   An electronic circuit, comprising:

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-        a chain of stream processing circuits (10a-c), mutually coupled to pass respective streams of sample values between pairs of successive stream processing circuits, at least part of the stream processing circuits (10a-c) having a control parameter input for receiving control parameter values;

5   -   a common control circuit (14) arranged to select block sizes of blocks of samples in the respective streams of a plurality of the stream processing circuits (10a-c), to select a control parameter value for each particular block and to transmit instructions specifying the selected block sizes and control parameter values;

-        a plurality of local control circuits (11), each coupled to the common control

10   circuit (14) and the control input of a respective corresponding stream processing circuit (10a-c) from the chain, each particular local control circuit (11) being arranged to receive at least part of the instructions and to apply parameter values from the instructions to its corresponding stream processing circuit (10a-c), the particular local control circuit (11) controlling timing of control parameter updates using block sizes from the instructions by

15   counting off block size dependent time intervals between times points of successive control parameter updates.

5.   An electronic circuit according to claim 4 operative in periodic sample cycles, wherein the stream processing circuits (10a-c) are arranged to indicate in which of the sample

20   cycles new samples are produced, each particular local control circuit (11) comprising a respective counter (24) that determines a count representative of a number of new sample values that have been indicated since the preceding one of the time points for input to its corresponding stream processing circuit (10a-c), the local control circuit (11) being arranged to trigger an update of the control parameters when said count represents a block size

25   specified in an instruction from the common control circuit (14).

6.   An electronic circuit according to claim 5, wherein the local control circuit (11) comprises a sample buffer (26) between its corresponding stream processing circuit (10a-c) and a supply source of input samples for the corresponding stream processing circuit,

30   said counter (24) counting new sample values at an input of the sample buffer (26), the sample buffer (26) delaying supply of new samples to the corresponding stream processing circuit (10a-c) by at least one processing cycle with respect to a processing cycle in which the new sample values are used to update the count.

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7.   An electronic circuit according to claim 5, wherein at least one of the local
control circuits (11) comprises a FIFO instruction buffer (22) arranged to buffer items of
instruction information received from the common control circuit (14), each item comprising
a control parameter value specification and a block size specification, said at least one of the
5   local control circuits (11) being arranged to apply the control parameter values specified by
successive items from the FIFO instruction buffer (22) successively to its corresponding
stream processing circuit (10a-c), the time interval after which the control parameter value of
the item is replaced by an update being selected by counting off the length of a time interval
specified by the block size specified by the item.

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8.   An electronic circuit according to claim 5, wherein at least one of the local
control circuits (11) comprises a look-up table memory (30) for storing a plurality of control
parameters values for its corresponding stream processing circuit (10a-c), the look-up table
memory (30) having a stored data output coupled to the control parameter input of the
15   corresponding stream processing circuit (10a-c) of the at least one of the local control circuits
(10a-c), the instructions from the common control circuit (14) containing identifications of
addresses in the look-up table memory (30), the at least one of the local control circuits (11)
addressing the look-up table memory (30) using the identifications.

20   9.   An electronic circuit according to claim 5, comprising a receiver circuit (9) for
receiving frames of a communication signal, the receiver circuit (9) comprising a detector for
detecting starting points of frames, the receiver circuit (9) being arranged to generate an input
stream of sample values for the chain, and reset signals each in a predetermined time relation
to a respective one of the starting points, the reset signals being fed to the local control
25   circuits (11), the local control circuits resetting (11) the counts in response to the reset signal.